

Appl. No. 09/736,225
Amendment dated: July 21, 2003
Reply to OA of: April 24, 2003

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-30 (canceled).

31(currently amended). A single semiconductor package consisting of an unsupported single layer linearly consisting of at least two solder mask portions formed at selected locations, and between and adjacent said solder mask portions is a die pad portion of said layer contiguous to each solder mask portion; and lead portions of said layer adjacent to and contiguous to said solder mask portions, said die pad portion has a chip adhering to the die pad surface; a plurality of conductive elements are electrically connecting the chip and the lead portion of the layer; and a molded resin covering the chip, conductive elements, solder ~~masks~~ mask portions, lead portion of the layer and die pad layer.

32(previously added). The semiconductor package of claim 31, wherein the solder mask is made from photosensitive and insulative materials selected from the group consisting of polyimide and ultraviolet-curable resins.

33(previously added). The semiconductor package of claim 32, wherein the lead layer and die pad layer are made of conductive materials selected from the group consisting of nickel and gold.

34(previously added). The semiconductor package of claim 32, wherein the solder mask is formed by performing photolithography process on a polyimide or ultraviolet-curable resin layer.

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35(previously added). The semiconductor package of claim 31, wherein the lead layer and die pad layer are formed by plating.

36(previously added). The semiconductor package of claim 31, wherein the conductive elements are made of a material selected from the group consisting of gold, copper and aluminum.

37(previously added). The semiconductor package of claim 31, wherein the die pad layer is replaced by a solder mask.

Claim D,
38(currently amended). A single semiconductor package consisting essentially of an unsupported single layer linearly consisting essentially of at least two solder mask portions formed at selected locations, and between and adjacent said solder mask portions is a die pad portion of said layer contiguous to each solder mask portion; and lead portions of said layer adjacent to and contiguous to said solder mask portions, said die pad portion has a chip adhering by a silver paste to the die pad surface; a plurality of conductive elements are electrically connecting the chip and the lead portion of the layer; and a molded resin covering the chip, conductive elements, solder ~~masks~~ mask portions, lead layer and die pad portion of the layer.

39(previously added). The semiconductor package of claim 38, wherein the solder mask is made from photosensitive and insulative materials selected from the group consisting of polyimide and ultraviolet-curable resins.

40(previously added). The semiconductor package of claim 38, wherein the lead layer and die pad layer are made of conductive materials selected from the group consisting of nickel and gold.

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41(previously added). The semiconductor package of claim 38, wherein the solder mask is formed by performing photolithography process on a polyimide or ultraviolet-curable resin layer.

42(previously added). The semiconductor package of claim 38, wherein the lead layer and die pad layer are formed by plating.

43(previously added). The semiconductor package of claim 38, wherein the conductive elements are made of a material selected from the group consisting of gold, copper and aluminum.

44(previously added). The semiconductor package of claim 38, wherein the die pad layer is replaced by a solder mask.

45(new). The semiconductor package of claim 31, wherein at least one side of the unsupported single layer has a surface which is coplanar.

46(new). The semiconductor package of claim 38, wherein at least one side of the unsupported single layer has a surface which is coplanar.